REMARKS/ARGUMENTS

1.) Amendments

Claims 18-20 have been cancelled without prejudice or disclaimer. Accordingly, claims 11-17 remain pending in the application.

2.) Claim Rejections – 35 U.S.C. §102(b)

The Examiner rejected claims 11-20 as being anticipated by Doblar, *et al.* (US 6,194.969). The Applicants traverse the claim rejections.

First, it is to be remembered that anticipation requires that the disclosure of a single piece of prior art reveals **every** element, or limitation, of a claimed invention. Furthermore, the limitations that must be met by an anticipatory reference are those set forth in each statement of function in a claims limitation, and such a limitation cannot be met by an element in a reference that performs a different function, even though it may be part of a device embodying the same general overall concept. Whereas Doblar fails to anticipate each and every limitation of claim 11, claim 11 is not anticipated thereby.

Claim 11 recites:

> 11. A computer system clocking system, said system comprising:
>
> at least two units with clock functionality, the units being coupled to a common system clock line, a common internal clock line, and a logic bus, wherein one unit is dedicated as a master unit at a time, the dedication of the master unit being dependent on at least a signal being given so as not to select a given unit for being a master unit, and if a given unit is dedicated as master unit when such a signal is given, the system performing a switchover causing another unit as the one not selected to be dedicated as master unit, each unit comprising:
>
> a clock source for generating a clock source signal, the clock source signal being adapted for being output on the internal clock line; and
>
> a phase lock loop device generating a signal, which is derived from the signal on the internal clock line, and which is output on the system clock line if the unit is dedicated as master unit, wherein one source clock signal of a unit is output on the internal clock line and all phase lock loop devices of all units generate phase lock loop output signals derived from the internal clock signal, the outputs of the phase lock loop devices being in phase with one another such that switchover from one phase lock loop output signal to another is seamless. (emphasis added).

Doblar does not disclose a common system clock line nor a common internal clock line. According to Doblar, clock signals from fan-out buffers 208A/B are individually provided to phase detector inputs of other devices. But no two units (105A, 105B) share a clock line: *i.e.*, no two units are hooked up on the same common clock line. The examiner asserts that the frequencies of each clock signal 106A 106B could be common. The frequencies, however, are not the decisive question, since a hardware "line" is what is recited in the claim. Thus, there must be a common clock line, which is not disclosed by Doblar.

The Examiner is not clear on what he interprets as the "internal clock line," which should be available to each unit according to claim 11. One possibility is fan-out buffer 106B; another possibility is fan-out buffers 208C/ 208D (leading to clock loads 350). The Examiner equates the system clock line with 106A from fan-out buffer 208A, and a phase lock loop device with Figure 3. Claim 11, however, states that each unit has a phase lock loop device. If Figure 3 of Doblar constitutes a phase lock loop device, it should be found in each unit, which is apparently not taught by Doblar – *i.e.*, only one Figure 3 device is expressly taught. Giving the broadest possible scope to the Examiner's reading of Doblar, however, it might be assumed that the clock board 105B constitutes a PLL of one unit, while Figure 3 constitutes a PLL of another unit. According to Applicants' invention recited in claim 11, however, the PLL (*e.g.*, 105B) of each unit should generate a signal which is derived form the signal on the internal clock line (*e.g.*, 208C). That, however, is not the case according to Dobblar. Furthermore, according to claim 11, the PLL signal is output on the system clock line (*e.g.*, 106A), which is also not taught by Dobblar. Therefore, even assuming a broad scope of the Examiner's reading of Doblar, Doblar fails to teach each and every limitation of claim 11. Claim 11, therefore, is not anticipated by Doblar.

With respect to the Examiner's rejection of claim 13, the Examiner's assertion that Doblar teaches that each unit comprises a first bidirectional port which communicates with the internal clock line (208C/D) is incorrect. Fan-out buffer outputs 208C or 208D are not bidirectional. Furthermore, the Examiner's assertion that Doblar teaches that each unit comprises a second bidirectional port which communicates with

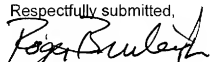
the system clock line (106A) is incorrect. The fan-out buffer outputs 105/106A are not bidirectional. Moreover, the Examiner's assertion that Doblar teaches to input or output respective system clock signals and respective internal clock signals is not correct. Fan-out buffer outputs 105A/106A are permanently output, and fan-out buffer outputs 208C/D are permanently output and never input. The only control which is accomplished by enable signals is in select PLL 300, which is not taught to occur in each unit (as described hereinabove with respect to claim 11). Accordingly, Doblar further fails to anticipate claim 13. With respect to the Examiner's rejection of claim 14, signals 106A and 106B are not enable signals, but clock signals which are derived from respective clock sources (VCXO). Thus, Doblar also fails to anticipate claim 14. Furthermore, whereas claims 15-17 are dependent from claim 11, and include the limitations thereof, those claims are also not anticipated by Doblar.

CONCLUSION

In view of the foregoing amendments and remarks, the Applicants believe all of the claims currently pending in the Application to be in a condition for allowance. The Applicants, therefore, respectfully request that the Examiner withdraw all rejections and issue a Notice of Allowance for claims 11-17.

The Applicants request a telephonic interview if the Examiner has any questions or requires any additional information that would further or expedite the prosecution of the Application.

Respectfully submitted,



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